CLAIMS

1. Apparatus for enhancing debug capability in a multiprocessor circuit, comprising:

a plurality of processors arranged so that data advances from processor to processor during normal operation;

an advancement circuit, the advancement circuit enabling advancement of data among the processors in the event of failure of a processor; and

a data bypass circuit to pass the data past a failed one of the processors.

2. The apparatus as in claim 1, wherein said data bypass circuit further comprises:

a bypass register.

3. The apparatus as in claim 1, further comprising:

said plurality of processors arranged to process data as a pipeline.

4. The apparatus as in claim 1, further comprising:

said plurality of processors arranged to process data as a pipeline; and

a bypass register, said bypass register having a bit location for each processor of the pipeline, each bit location capable of storing an override signal.

5. The apparatus as in claim 1, further comprising:

a memory, said memory storing computer code, said computer code having a code entry point selected by said data bypass circuit to enable a downstream processor to do the work of a failed processor.

6. A method for enhancing debug capability in a multiprocessor circuit, comprising:

advancing data among a plurality of processors, the plurality of processors arranged so that data advances from processor to processor during normal operation;

advancing data among the processors by an advancement circuit, in the event of failure of a processor; and

passing the data past a failed one of the processors by a data bypass circuit.

7. The method apparatus as in claim 6, further comprising:

indicating that a processor is to be bypassed by a bypass register.

8. The method as in claim 6, further comprising:

arranging said plurality of processors to process data as a pipeline.

9. The method as in claim 6, further comprising:

arranging said plurality of processors to process data as a pipeline; and

storing an override signal in a bit location of a bypass register.

10. The method as in claim 6, further comprising:

storing computer code in a memory, said computer code having a code entry point selected by said data bypass circuit to enable a downstream processor to do the work of a failed processor.

11. Apparatus for enhancing debug capability in a multiprocessor circuit, comprising:

means for advancing data among a plurality of processors, the plurality of processors arranged so that data advances from processor to processor during normal operation;

means for advancing data among the processors by an advancement circuit, in the event of failure of a processor; and

means for passing the data past a failed one of the processors by a data bypass circuit.

12. The apparatus as in claim 11, further comprising:

means for indicating that a processor is to be bypassed by a bypass register.

13. The apparatus as in claim 11, further comprising:

means for arranging said plurality of processors to process data as a pipeline.

14. The apparatus as in claim 11, further comprising:

means for arranging said plurality of processors to process data as a pipeline; and

storing an override signal in a bit location of a bypass register.

15. The apparatus as in claim 11, further comprising:

means for storing computer code in a memory, said computer code having a code entry point selected by said data bypass circuit to enable a downstream processor to do the work of a failed processor.

16. A computer readable media, comprising:

said computer readable media having instructions written thereon for execution on a processor for the practice of the method of claim 6.

17. Electromagnetic signals propagating on a computer network, comprising:

said electromagnetic signals carrying instructions for execution on a processor for the practice of the method of claim 6.